CLAIMS

What is claimed is:

1. A nonlinearity detection system for an analog to digital converter (ADC), comprising:

a triangular wave generator that generates a triangular wave that is output to the ADC;

a differentiator module that communicates with the ADC and that generates an output signal that is based on an output of the ADC and a delayed output of the ADC; and

a nonlinearity detection module that detects slope discontinuities in said output signal of said differentiator module.

2. The nonlinearity detection system of Claim 1 wherein said differentiator module includes a discrete-time differentiator.

3. The nonlinearity detection system of Claim 1 wherein said differentiator module includes a discrete time filter.

4. The nonlinearity detection system of Claim 3 wherein said discrete time filter includes a finite impulse response (FIR) filter.

5. An integrated circuit comprising the nonlinearity detection system of Claim 1 and further comprising said ADC.

6. The nonlinearity detection system of Claim 1 wherein said nonlinearity detection module determines maximum and minimum positive and negative slope limits for positive and negative slope regions, respectively, of said output signal of said differentiator module.

7. The nonlinearity detection system of Claim 6 wherein said nonlinearity detection module compares slope values in said positive slope region to said maximum and minimum positive slope limits to detect said slope discontinuities.

8. The nonlinearity detection system of Claim 7 wherein said nonlinearity detector generates a nonlinearity test fail signal when said slope values in said positive slope region are at least one of greater than said maximum positive slope limit and less than said minimum positive slope limit during said positive slope regions.

9. The nonlinearity detection system of Claim 6 wherein said nonlinearity detection module compares slope values in said negative slope regions to said maximum and minimum negative slope limits to detect said slope discontinuities.

10. The nonlinearity detection system of Claim 9 wherein said nonlinearity detection module generates a nonlinearity test fail signal when said slope values in said negative slope regions are at least one ofgreater than said maximum negative slope limit and less than said minimum negative slope limit during said negative slope regions.

11. The nonlinearity detection system of Claim 1 wherein said nonlinearity detection module comprises:

a slope region identifying module that identifies positive and negative slope regions in said output signal of said differentiator module;

a positive slope limit module that determines maximum and minimum limits for said positive slope region;

a negative slope limit module that determines maximum and minimum limits for said negative slope region; and

a comparing module that receives said output signal of said differentiator module, that compares said output signal of said differentiator module to one of said maximum and minimum limits for said positive slope region and said maximum and minimum limits for said negative slope region, and that generates a nonlinearity test signal based on said comparison.

12. The nonlinearity detection system of Claim 7 wherein said nonlinearity detector generates a nonlinearity test pass signal when said slope values in said positive slope region are at least one of less than said maximum positive slope limit and greater than said minimum positive slope limit during said positive slope regions.

13. The nonlinearity detection system of Claim 9 wherein said nonlinearity detection module generates a nonlinearity test pass signal when said slope values in said negative slope regions are at least one of less than said maximum negative slope limit and greater than said minimum negative slope limit during said negative slope regions.

14. An integrated circuit comprising the nonlinearity detection system of Claim 1.

15. An Ethernet physical layer device comprising the nonlinearity detection system of Claim 1.

16. The Ethernet physical layer device of Claim 15 wherein said Ethernet physical layer device is compatible with 1000BaseT.

17. A nonlinearity detecting system for an analog to digital converter (ADC), comprising:

triangular wave generating means for generating a triangular wave that is output to the ADC;

differentiating means that communicates with the ADC for generating an output signal that is based on an output of the ADC and a delayed output of the ADC; and

nonlinearity detecting means for detecting slope discontinuities in said output signal of said differentiating means.

18. The nonlinearity detecting system of Claim 17 wherein said differentiating means includes a discrete-time differentiator.

19. The nonlinearity detecting system of Claim 17 wherein said differentiating means includes a discrete time filter.

20. The nonlinearity detecting system of Claim 19 wherein said discrete time filter includes a finite impulse response (FIR) filter.

21. An integrated circuit comprising the nonlinearity detecting system of Claim 17 and further comprising said ADC.

22. The nonlinearity detecting system of Claim 17 wherein said nonlinearity detecting means determines maximum and minimum positive and negative slope limits for positive and negative slope regions, respectively, of said output signal of said differentiating means.

23. The nonlinearity detecting system of Claim 22 wherein said nonlinearity detecting means compares slope values in said positive slope region to said maximum and minimum positive slope limits to detect said slope discontinuities.

24. The nonlinearity detecting system of Claim 23 wherein said nonlinearity detecting means generates a nonlinearity test fail signal when said slope values in said positive slope region are at least one of greater than said maximum positive slope limit and less than said minimum positive slope limit during said positive slope regions.

25. The nonlinearity detecting system of Claim 22 wherein said nonlinearity detecting means compares slope values in said negative slope regions to said maximum and minimum negative slope limits to detect said slope discontinuities.

26. The nonlinearity detecting system of Claim 25 wherein said nonlinearity detecting means generates a nonlinearity test fail signal when said slope values in said negative slope regions are at least one of greater than said maximum negative slope limit and less than said minimum negative slope limit during said negative slope regions.

27. The nonlinearity detecting system of Claim 17 wherein said nonlinearity detecting means comprises:

slope region identifying means for identifying positive and negative slope regions in said output signal of said differentiating means;

positive slope limit means for determining maximum and minimum limits for said positive slope region;

negative slope limit means for determining maximum and minimum limits for said negative slope region; and

comparing means that receives said output signal of said differentiating means for comparing said output signal of said differentiating means to one of said maximum and minimum limits for said positive slope region and said maximum and minimum limits for said negative slope region, and for generating a nonlinearity test signal based on said comparison.

28. The nonlinearity detecting system of Claim 23 wherein said nonlinearity detecting means generates a nonlinearity test pass signal when said slope values in said positive slope region are at least one of less than said maximum positive slope limit and greater than said minimum positive slope limit during said positive slope regions.

29. The nonlinearity detecting system of Claim 25 wherein said nonlinearity detecting means generates a nonlinearity test pass signal when said slope values in said negative slope regions are at least one of less than said maximum negative slope limit and greater than said minimum negative slope limit during said negative slope regions.

30. An integrated circuit comprising the nonlinearity detecting system of Claim 17.

31. An Ethernet physical layer device comprising the nonlinearity detecting system of Claim 17.

32. The Ethernet physical layer device of Claim 31 wherein said Ehternet physical layer device is compatible with 1000BaseT.

33. A method for detecting nonlinearity in an analog to digital converter (ADC), comprising:

generating a triangular wave that is output to the ADC;

generating an output signal that is based on an output of the ADC and a delayed output of the ADC; and

detecting slope discontinuities in said output signal.

34. The method of Claim 33 wherein said step of generating said output signal includes performing discrete-time differentiation.

35. The method of Claim 33 wherein said step of generating said output signal includes performing discrete time filtering.

36. The method of Claim 35 wherein said discrete time filtering includes finite impulse response (FIR) filtering.

37. The method of Claim 33 further comprising determining maximum and minimum positive and negative slope limits for positive and negative slope regions, respectively, of said output signal.

38. The method of Claim 37 further comprising comparing slope values in said positive slope region to said maximum and minimum positive slope limits to detect said slope discontinuities.

39. The method of Claim 38 further comprising generating a nonlinearity test fail signal when said slope values in said positive slope region are at least one of greater than said maximum positive slope limit and less than said minimum positive slope limit during said positive slope regions.

40. The method of Claim 37 further comprising comparing slope values in said negative slope regions to said maximum and minimum negative slope limits to detect said slope discontinuities.

41. The method of Claim 40 further comprising generating a nonlinearity test fail signal when said slope values in said negative slope regions are at least one of greater than said maximum negative slope limit and less than said minimum negative slope limit during said negative slope regions.

42. The method of Claim 33 further comprising:

identifying positive and negative slope regions in said output signal;

determining maximum and minimum limits for said positive slope region;

determining maximum and minimum limits for said negative slope region;

comparing said output signal to one of said maximum and minimum limits for said positive slope region and said maximum and minimum limits for said negative slope region; and

generating a nonlinearity test signal based on said comparison.

43. The method of Claim 40 further comprising generating a nonlinearity test pass signal when said slope values in said positive slope region are at least one of less than said maximum positive slope limit and greater than said minimum positive slope limit during said positive slope regions.

44. The method of Claim 40 further comprising generating a nonlinearity test pass signal when said slope values in said negative slope regions are at least one of less than said maximum negative slope limit and greater than said minimum negative slope limit during said negative slope regions.